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Battery-Less Electroencephalogram System Architecture Optimization

by Peter Gadfort and Renooka Karmarkar

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Battery-Less Electroencephalogram System Architecture Optimization

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This report presents a new self-powered architecture to enable real-world recording of electroencephalograms, which will enable research-grade recording outside of the laboratory setting. The system operates on just 1% of the power of a regular full-powered system, which makes it possible to power it from a power-harvesting scheme using a thermoelectric generator. This work presents a comparison of several different versions of this architecture and analysis of the major design parameters available to the circuit designers to determine the best parameters to impact the performance (power and recording fidelity) of the system.

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Contents

1. Introduction **1**

1.1 Background 1

1.2 Commercial Systems 2

2. System Design **3**

2.1 System Power 4

2.2 Proposed System Architecture 5

2.3 DSP Decision Rules 6

2.3.1 Rule 1 – Gain Determination 6

2.3.2 Rule 2 – Voltage Offset Determination 6

2.3.3 Rule 3 – Bitdepth Determination 7

3. Experimental Setup **8**

3.1 Architectures Under Consideration 9

3.2 Power Modeling 9

4. Results and Discussion **10**

4.1 Effects of Different Architectures 10

4.2 Effects of Channel Count 12

4.3 Effects of AFE Adjustment Frequency 14

4.4 Effects of Major AFE Parameters 15

4.4.1 VOC Resolution 15

4.4.2 ADC Resolution 17

4.4.3 Bandwidth 20

4.4.4 Noise 21

4.4.5 Sampling Frequency 22

5. Conclusions **22**

6. References **24**

List of Symbols, Abbreviations, and Acronyms **25**

Distribution List **26**

List of Figures

Fig. 1 Sample EEG measurements....2
Fig. 2 Common EEG architecture 2
Fig. 3 Proposed EEG system....5
Fig. 4 Required bitdepths for ADC vs. gain and resolution....7
Fig. 5 Selected architectures for modeling 9
Fig. 6 Sample simulation power breakdown for architecture 4 12
Fig. 7 Performance impacts of channel count 13
Fig. 8 Performance impacts of F_{adjust} 14
Fig. 9 Performance impacts of VOC resolution 15
Fig. 10 VOC offset voltages for various resolutions 17
Fig. 11 Performance impacts of ADC resolution 18
Fig. 12 ADC bitdepths selected 19
Fig. 13 LNA gain settings 19
Fig. 14 Performance impacts of LNA and MUX bandwidth 21
Fig. 15 Performance impacts of VOC, LNA, MUX, and ADC noise 21
Fig. 16 Performance impacts of sampling frequency 22

List of Tables

Table 1 Sample specifications of commercial systems/products 3
Table 2 Power model parameters 10
Table 3 Performance of different architectures from Fig. 5 10
Table 4 ADC bitdepth summary 20

1. Introduction

The recording and analysis of brain activity is of great interest to those studying the brain and brain disorders, especially in real-world situations, such as when a Soldier is in theater.

There are several methods to study the electrical activity in the brain, such as electrocorticography (ECoG) and electroencephalogram (EEG), with varying degrees of invasiveness and accuracy. Because ECoG is very invasive, requiring surgery to implant the electrodes, this technique is ill suited for mass deployment of neural recorders. EEGs are a noninvasive method to measure the electrical activity in the brain that can still be used to study brain activity.

Currently, most EEGs are recorded in highly controlled laboratory environments, which control for the electromagnetic interference of equipment, ambient radio signals, and the patient's movements. This type of control would not be possible to replicate in the field, as Soldiers would be moving around. Additionally, for a fieldable system, the implementation of the EEG cannot impede the Soldier, and therefore, the size and weight of the EEG system would need to be designed to account for this.

This report outlines the architectural decisions required to redesign the EEG system architectures to address the power and practical recording considerations required to design a system that can be used by the Soldier.

1.1 Background

Current commercial EEG systems are not useful for the Army's purposes. Commercial systems are targeted for either scientific research or consumer-grade electronics. Neither of these 2 categories can satisfy the Army's needs, as the scientific equipment is much too heavy and cumbersome for a Soldier to wear in the field and consumer-grade electronics are not designed with sufficient accuracy to permit meaningful research on the data. Furthermore, neither set of systems can meet the power requirements for a 72-h mission.

The EEG system desired to achieve this task must amplify a target signal with a resulting minimum resolution below 1 μV while handling 10- to 100-mV swings generated by head movements, eye blinks, and other motion artifacts along with

any generated environmental noise. Figure 1 depicts an example of a 16-channel EEG signal recorded for 10 s. These signals have already been processed to remove the artifacts and therefore look relatively clean.

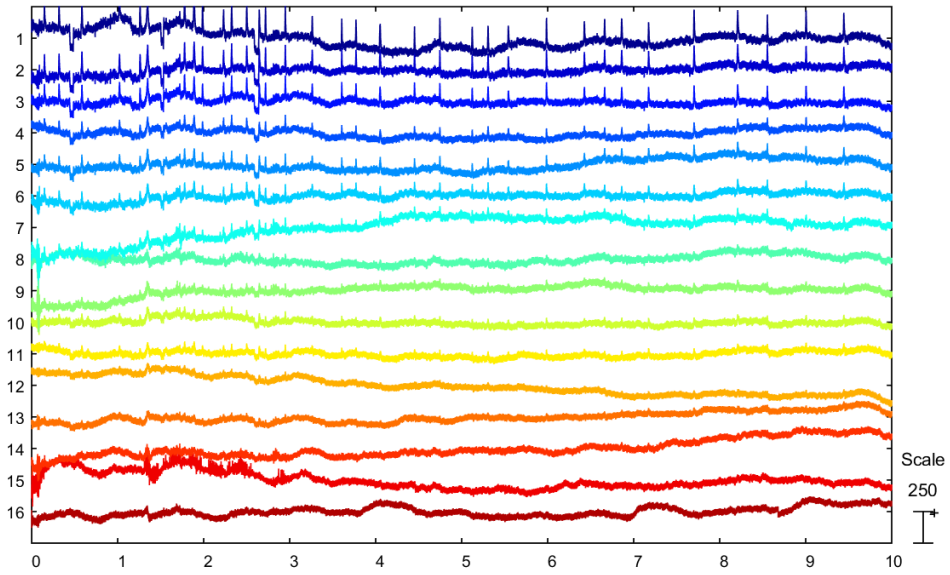


Fig. 1 Sample EEG measurements

Figure 2 shows an example of a typical EEG system, which includes a low-noise amplifier (LNA), data converters, and an radio frequency (RF) link to transmit the data to some host system. This work focuses on the analog frontend (AFE) and digital systems from Fig. 2 and leaves the RF link and host for future work.

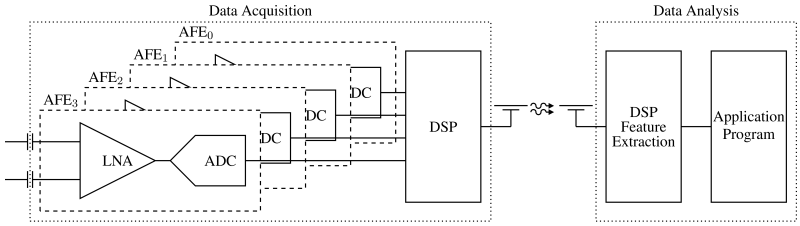


Fig. 2 Common EEG architecture

1.2 Commercial Systems

The performance specifications of 2 commercially available systems have been tabulated in Table 1. Both of the full commercial systems would not be suitable for

Soldier applications, since the battery life is not suitable for a nominal 72-h mission; therefore, these systems would require several recharges over that mission, which would add weight to the Soldier's load. The third product in the table is a commercial chip from Texas Instruments.[1] While this is not a full system, it would be possible to use this as a base to build a larger system as its power consumption would allow it to operate from a AA battery for more than 72 h. While this might be acceptable in commercial applications, the Soldier already carries tens of pounds of batteries and this EEG system should not add to that load.

Table 1 Sample specifications of commercial systems/products

	EMOTIV Epoc+[2]	Neuroelectronics ENOBIO[3]	TI ADS1299[1]
Channels	14	8, 20, or 32	8
Bandwidth	0.2–43 Hz	0–250 Hz	27–662 kHz
Samples per second	256	500	250 – 16k
Resolution	0.51 µV	0.05 µV	0.72 µV
Noise	N/A	< 1 µV RMS	1 µV VPP
Battery life	6 – 12 h	13 – 16 h	40 mW (97.5 h)

2. System Design

To archive an EEG system that can be worn by the Soldier in the field, there are several requirements the system must meet:

1) The system should not add to the weight the Soldier is carrying; therefore, it will need to be self-powered (Section 2.1).

2) The system must be able to amplify the signal with minimal distortion due to negligible clipping and other nonlinearity problems (Section 2.2).

3) The system will need to be intelligent enough to be able to balance the recording quality and power requirements (Section 2.3).

The following sections cover the general approach to satisfy each of the previous criteria.

2.1 System Power

One of the main concerns while designing an EEG system architecture that needs to be self-powered is the power consumption and preservation, as the energy required to power the system will need to be harvested from the environment. There are several methods to harvest power from RF, solar, motion, and thermal. In this case, thermal energy harvesting appears to be the most promising.

A thermoelectric generator (TEG) should be able to harvest enough energy from the heat of the Soldier's scalp to enable the EEG system. Based on the work of Carmo et al.,[4] a TEG would be able to provide between 100–500 $\mu W\,cm^{-2}$ with a 1-K temperature gradient. Based on this estimate, the system would be able to operate on a power budget of 200–300 μW, which keeps the TEG relatively small while providing a realistic target size of several square centimeters. The size could be as small as 0.4 cm^2 and as large as 3 cm^2.

Because of the limited power budget, the system will be operating in subthreshold (SubVt), which will support the low-power operation required, but places many requirements on the AFE. In SubVt, the operating voltages of the system are reduced to below 1 V from the usual 5 V,[1] which allows for a 25× to 125× reduction in power. However, because of the reduced voltages, the input voltage range will be limited and additional circuits will be required to maintain a recordable signal. Therefore, a voltage offset controller (VOC) will be introduced to stabilize the LNA; otherwise, the system would risk major signal distortions due to clipping in the amplifiers.

The power budget of 300 μW would need to be distributed across several subsystems, such as the AFE, data converters, digital signal processor, and wireless telemetry. Since the wireless telemetry is not being considered in this work, 100 μW will be allocated to its power budget.[5] Therefore, only 100–200 μW would be available to the frontend and signal processing.

2.2 Proposed System Architecture

The proposed EEG architecture, shown in Fig. 3, notionally contains 4 AFEs each with a VOC, LNA, and variable gain amplifier (VGA). However, the number of channels can be increased or decreased based on need. The 4 channels are time multiplexed together in the multiplexer (MUX) and fed to the analog-to-digital converter (ADC) to be digitized. The digitized data are then provided to the digital signal processor (DSP), which will process the data and determine the appropriate settings for each AFE.

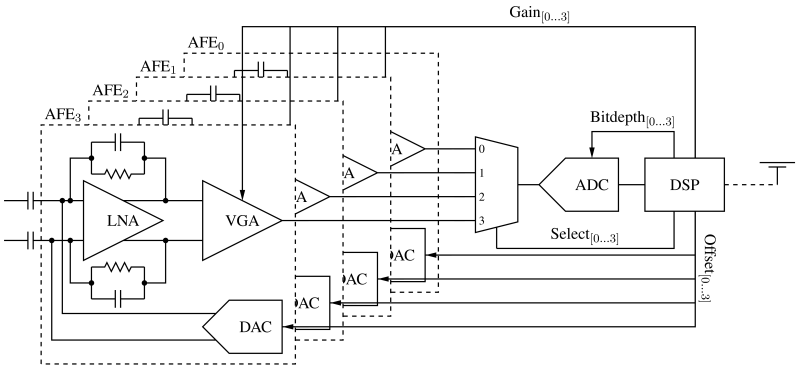


Fig. 3 Proposed EEG system

This setup is intended to operate at low voltages to save power. However, this poses some challenges with keeping the LNA and VGA from clipping the incoming signals, due to the reduced input voltage range of the LNA. To overcome this, the VOC/digital-to-analog converters (DACs) are added to compensate for the DC voltage offset, which effectively extends the input range of the LNA.[6]

The VGAs and LNAs are responsible for setting the noise floor of the system and should therefore be set to have the highest gain possible without causing distortion to the signal. Finally, the ADC has a variable bitdepth,[7] which allows the system to reduce the power required for the data conversions, if additional resolution and dynamic range are not required. Each of these components can be controlled by the DSP, which will analyze the signal and determine the appropriate settings for the VOC, LNA, and ADC to maximize signal fidelity and minimize power. This feedback and controllable settings of the AFE makes this an adaptive data acquisition (ADA) system. The rules used in this work are expanded upon in Section 2.3.

2.3 DSP Decision Rules

Although the DSP would be capable of sophisticated calculations and rules, for the purposes of this work, several simple rules have been devised. Examples of potentially more powerful rules would include rules that can proactively handle eye blinks and muscle movements, which tend to be high amplitude and would require additional processing to correct for these effects.

2.3.1 Rule 1 – Gain Determination

1) Determine allowable system input min, max, and peak-to-peak values:
   (a) Compute $\text{gain}_0 = \frac{\text{input}_{\text{min}}}{\text{signal}_{\text{min}}}$. This checks the maximum gain possible on the negative rail.
   (b) Compute $\text{gain}_1 = \frac{\text{input}_{\text{max}}}{\text{signal}_{\text{max}}}$. This checks the maximum gain possible on the positive rail.
   (c) Compute $\text{gain}_2 = \frac{\text{input}_{\text{pp}}}{\text{signal}_{\text{pp}}}$. This checks the maximum gain possible for the differential signal.
2) Determine minimum gain from gain_0, gain_1, and gain_2, which will guarantee that the system does not clip the signal.
3) Lookup the gain in gain table and apply the setting.

2.3.2 Rule 2 – Voltage Offset Determination

1) Take the old offset value and scale to the new AFE gain.
2) Determine if the signal is clipped:
   (a) If yes, offset the signal by V_{DD} towards the clipping.
   (b) If no, offset the signal by the last value of the signal. This is acting as a proxy for the DC value of the signal. The mean of the signal would also have been a good candidate; however, this would have required additional processing by the DSP, which would have increased the DSP power.
3) Apply the offset.

2.3.3 Rule 3 – Bitdepth Determination

To determine the bitdepth the following 2 equations are used:

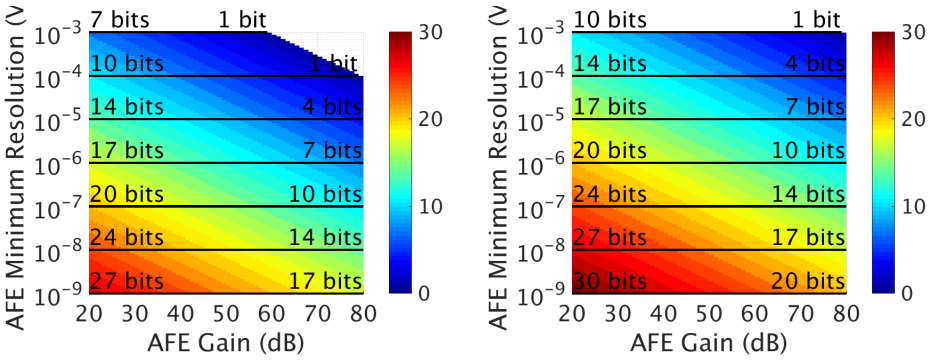
$$\mathrm{V}_{\mathrm{min}} = \frac{\mathrm{V}_{\mathrm{swing}}}{10^{\frac{G}{20}} \times 2^{N}} \tag{1}$$

$$N = \left\lceil \log_2 \mathrm{V}_{\mathrm{swing}} - \log_2 \mathrm{V}_{\mathrm{min}} - G \times \frac{\log_2 10}{20} \right\rceil \tag{2}$$

where $\mathrm{V}_{\mathrm{min}}$ is the system resolution, $\mathrm{V}_{\mathrm{swing}}$ is the input swing of the data converter, G is the gain in dB, and N is the bitdepth. Equation 1 is used to compute the minimum resolution the designer is interested in and Eq. 2 solves Eq. 1 for N.

The following steps are used in the bitdepth determination:

1) Take the new gain of the AFE.
2) Compute Eq. 2 to determine N based on the desired resolution. The bitdepth ranges for specific desired resolutions based on this equation are shown in Fig. 4.
3) Look up N in the bitdepth list and apply to the ADC.



(a) $\mathrm{V}_{\mathrm{swing}}$ = 1 V **(b) $\mathrm{V}_{\mathrm{swing}}$ = 10 V**

Fig. 4 Required bitdepths for ADC vs. gain and resolution

While the system is running, $\mathrm{V}_{\mathrm{swing}}$ will be held constant and for this work $\mathrm{V}_{\mathrm{min}}$ will as well. Therefore, only the gain will determine the bitdepth. In more sophisticated rules, $\mathrm{V}_{\mathrm{min}}$ could possibly be modified to account for the current needs of the system.

From Fig. 4, it is apparent that lowering the input swing to the ADC also reduces the number of bits required to achieve a given resolution, which makes sense based on Eq. 2, but this also helps save power because power will be proportional to 2^N. This system will be targeting 1 µV with a ±500-mV swing, which means the required bitdepths for the ADC are 7 to 17 bits based on the assumed AFE gain (Fig. 4a).

3. Experimental Setup

To analyze the effects of this system on signal fidelity and power, tests on different system setups as well as systems of varied settings (i.e., gain, bitdepth, and voltage offset) have been performed. This work presents a tradeoff analysis of several different architectures and discusses how each impacts power and signal fidelity, compared to a baseline regular system without the ADA enabled.

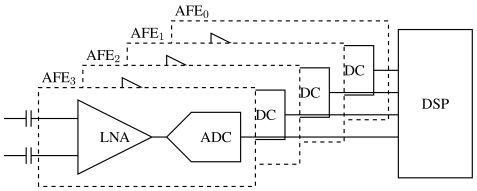
The goal of this experiment is to show that the ADA does not impact the fidelity of the signal. This is accomplished by comparing the output of a baseline system, which does not include the ADA, with different systems with the ADA enabled.

Section 4.1 presents the analysis of the different architectures in Section 3.1. Section 4.2 presents an analysis of the impact the number of channels has on the system. Section 4.3 presents an analysis of the impact the DSP adjustment rate has on the frontend. Section 4.4 presents an analysis of the different component parameters to aid in the circuit design of the system.

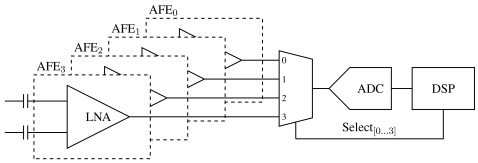
To accurately model the system power and fidelity, a MATLAB model was developed to allow for the design-space exploration. This allows for a cycle accurate model, which can predict the effects of switching the AFE settings and track the power required. The data used to evaluate the efficacy of the different architectures were previously recorded EEG data sets, which were upsampled to provide enough samples for the model to process.

3.1 Architectures Under Consideration

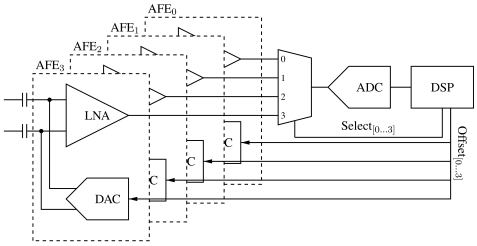
The architectures under consideration are presented in Fig. 5. Figure 5a serves as the baseline system, as it is comparable to the Texas Instruments ADS1299.[1] The remaining systems build upon the previous one, to show the impact of each additional control, shown in Fig. 5b–e.



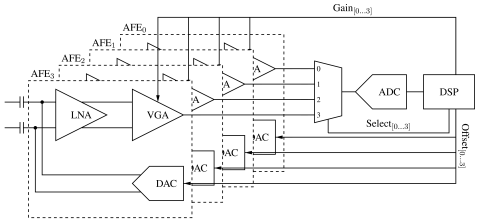
(a) Architecture 0: Baseline



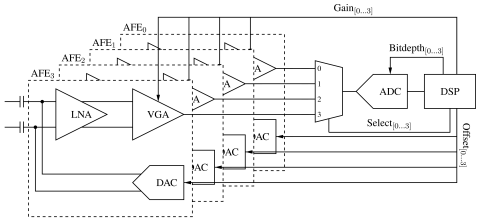
(b) Architecture 1: Architecture 0 with MUX



(c) Architecture 2: Architecture 1 with offset controller



(d) Architecture 3: Architecture 2 with gain controller



(e) Architecture 4: Architecture 3 with bitdepth controller

Fig. 5 Selected architectures for modeling

3.2 Power Modeling

To model the power in these architectures, the MATLAB model used the parameters in Table 2, which were derived from the sources listed. The power is broken into 2 sources, static and dynamic. Static is the power the component consumes regardless of the state of the settings and dynamic is dependent on the settings and operations of the system. The loading capacitance for the MUX is overestimated, but overall

the MUX does not contribute much to the total power, so this did not result in a large error.

Table 2 Power model parameters

	Static	Dynamic
LNA[8]	680 nW V^{-1}	0
ADC[7]	25.5 µW V^{-1}	$2^N \times 50.2$ fJ/sample
MUX[7]	1.50 µW V^{-1}	1 pF $\times V_{DD}^2$
VOC[7]	3.00 µW V^{-1}	$2^N \times 50.2$ fJ/sample
DSP[9]	1.67 µW V^{-1}	11.7 pJ/add & 187.2 pJ/multiply

4. Results and Discussion

4.1 Effects of Different Architectures

The results of the different systems, shown in Fig. 5, have been tabulated in Table 3. The first architecture serves as the baseline for comparisons. This was modeled at 5 V with 4 channels, which yields a very good signal fidelity, but would not be able to meet the desired system power budget.

Table 3 Performance of different architectures from Fig. 5

Architectures	RMS Error (%)		Power (µW)	Waste (µW)
	Mean	STDEV		
0 (Baseline)	0.04	0.10	3978.37	2.03
1	1.17	2.69	3603.58	53.15
1 reduced V_{DD}	52.63	26.10	19.09	3.42
2	0.66	0.27	25.63	0.05
3	0.81	0.63	25.90	0.07
4	0.81	0.62	26.84	0.07

Introducing the analog MUX allows the system to share particularly power-hungry subsystems such as the ADC. In architecture 1, the power is reduced by a little under 10%, by allowing the 4 channels to share the ADC. While this removes 3 ADCs from the system, it does require the remaining ADC to operate at 4 times the

sampling rate to gather the same data, which accounts for the diminished reduction. However, this does come with some negative tradeoffs, such as a decrease in the fidelity, which is due to the MUX channel crosstalk; this is further explored in Section 4.4.3. However, overall this does improve power and reduces the silicon footprint of the ADC, which are both desirable outcomes.

Bringing that architecture down to SubVt, operating at 500 mV instead of 5 V, the operation results in unacceptable distortion of the signal; however, the power reduced by 99.5%. This distortion is due to the clipping of the input signal in the amplifiers, but this can be remedied with additional circuits, as shown.

The addition of the VOC brings the error below 1%, while meeting the power budget. This yields the first candidate system, which can meet the requirements laid out earlier in Section 2. With the addition of the gain and bitdepth controllers, the error remains near 1% with a minor impact on power, with a total of 4.7% increase. While the gain and bitdepth controls do not appear to offer much improvement at this stage, they have been left in since the data being used to characterize this setup do not include large swing effects like muscle movements and eye blinks.

As a proxy for system efficiency, the waste power is included in Table 3. The waste power is defined by Eq. 3, where $\text{Error}_{\text{RMS}}$ is the root mean square (RMS) error of the signal when compared to the original signal:

$$\text{P}_{\text{waste}} = \text{Error}_{\text{RMS}} \times \text{Power} \tag{3}$$

Ideally, this would be 0, but that is not practical; therefore, we target the systems with as small a waste as possible. While architecture 3 appears to be performing equivalently to architecture 4, the addition of the bitdepth control can be useful in other applications outside of the EEG. For the remainder of this work, architecture 4, shown in Fig. 5e, is considered.

Figure 6 shows the breakdown of power for each component in the system for architecture 4 with 4 channels. From this figure, it is apparent that the largest contributor to the power is the ADC, followed by the VOC. Both of these account for a total of 82% of the power. Therefore, each of these component must be carefully designed so that they do not overwhelm the total power budget in the system.

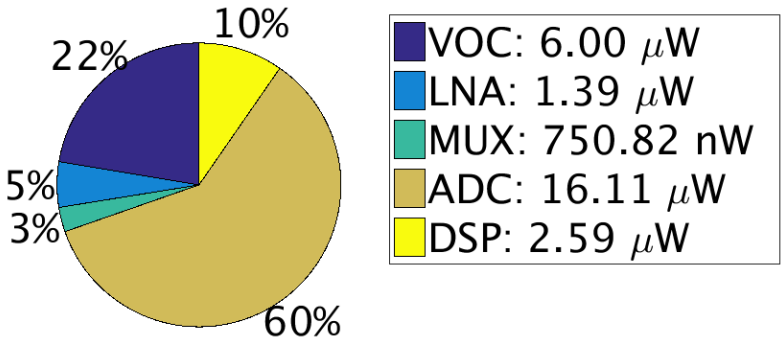
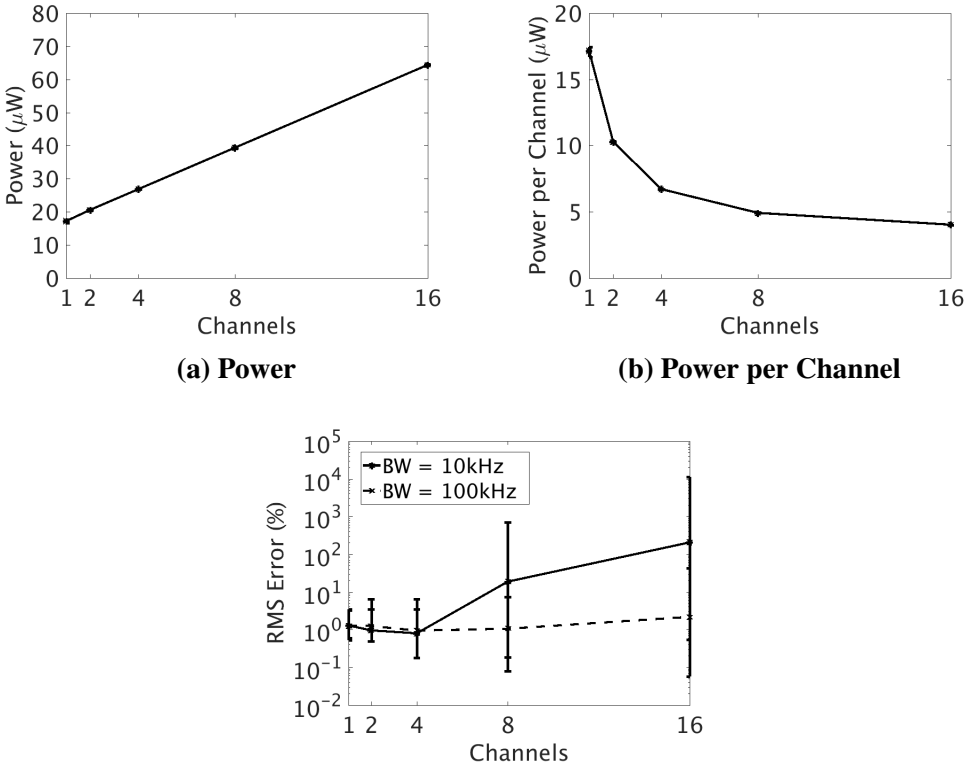


Fig. 6 Sample simulation power breakdown for architecture 4

4.2 Effects of Channel Count

As mentioned in Section 4.1, the most energy hungry device in the system is the ADC. Therefore, time multiplexing channels together, allowing them to share the ADC, helps drive the system efficiency up. This is apparent in Fig. 7b, where the power per channels drops by 73% going from a 1- to 16-channel system, while maintaining a total power, shown in Fig. 7a, well below the budget limits.



(a) Power **(b) Power per Channel**

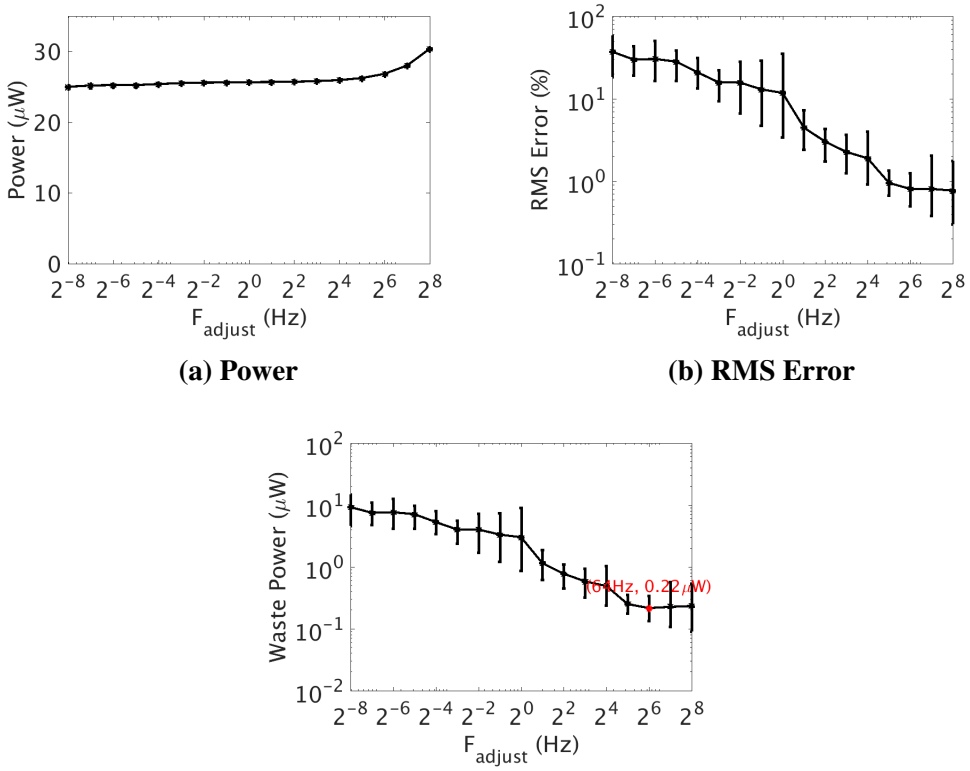
(c) RMS Error

Fig. 7 Performance impacts of channel count

Fig. 7a indicates a linear relationship between power and number of channels; therefore, extrapolating to the upper limits of the power budget of 200 µW, this system would be able to support 59 channels. However, this requires that the bandwidth of the MUX is sufficiently high to support the high switching speed. This limitation can be observed in Fig. 7c, where the RMS error increases dramatically going from 4 to 16 channels. To show that this is a manageable issue to overcome, the MUX bandwidth is modified to 100 kHz. This figure shows that the error decreases by several orders of magnitude when the bandwidth is increased. This is further explored in Section 4.4.3.

4.3 Effects of AFE Adjustment Frequency

What sets this system apart from other systems is its ability to dynamically adjust the system parameters based on the measured data. While this could be a continuous operation, it would likely be too computationally costly and only be worth it if the algorithms could make use of the information. Therefore, the optimum adjustment frequency is algorithm-dependent. Here the system is assumed to be operating on the algorithms provided in Section 2.3. Figure 8 shows the system performance while changing the adjustment frequency from 4 mHz to 256 Hz. As one would expect, the power, shown in Fig. 8a, is mildly dependent on the adjustment period, since the DSP is already modeled to be power efficient and the algorithms do not require much computation. This would not be the case for increasingly sophisticated algorithms.



(a) Power **(b) RMS Error**

(c) Waste Power

Fig. 8 Performance impacts of F_{adjust}

While the impact on power is small, the impact on the RMS error is substantial. This

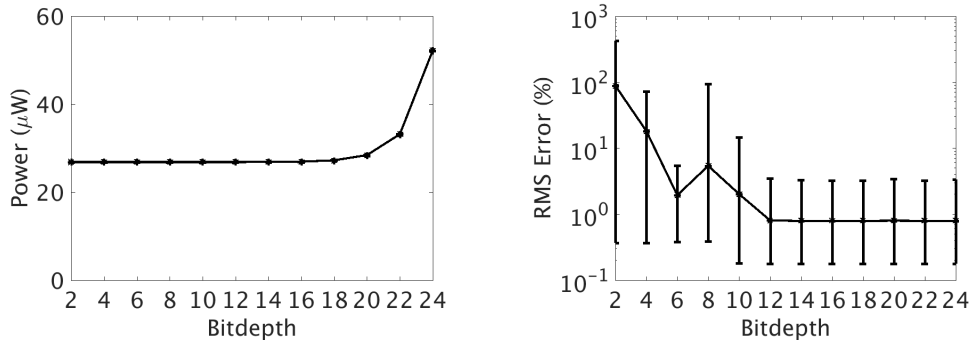
is due to the amplifier and VOC parameters not being adjusted frequently enough to prevent clipping of the signals. This is evident at the low adjustment frequencies in Fig. 8b; here the error approached 100% and the signal would be useless at these error levels. Therefore, the adjustment frequency needs to be high enough to capture the signal faithfully. To determine the adjustment frequency to use for the remainder of this work, the minimum wasted power parameter was used, as shown in Fig. 8c, which shows the minimum to occur at 64 Hz. At this frequency, the estimated power waste is 220 nW. Different algorithms would affect this and place different requirements on the adjustment frequency.

4.4 Effects of Major AFE Parameters

Each of the subsystems in this architecture will have a different impact on the overall performance. In the following sections, the major parameters of each subsystem are modified independently and their impacts evaluated. This will be useful for to determine which parameters will require special attention by the designer and which will have no measurable impact and can be ignored.

4.4.1 VOC Resolution

Since the VOC is helping the amplifier stay out of saturation, the resolution of this component must be high enough to make meaningful corrections while not consuming too much power. The performance impact is plotted in Fig. 9. While the bitdepth of the VOC is less than 18 bits, there is not a large impact on power, and the signal error only becomes acceptable above 12 bits. This would indicate that the bitdepth would need to be at least 12 bits but no more than 18 bits.



(a) Power **(b) RMS Error**

Fig. 9 Performance impacts of VOC resolution

Figure 10 shows the output voltage of the VOC for several bitdepths. From these plots, it is evident that below 12 bits the VOC is too discretized to be effective, and above 14 bits the outputs are about the same. It should be noted that the total swing of the VOC is the full $\pm 500\,\mathrm{mV}$, which does not appear to be required as the values all fall between $\pm 25\,\mathrm{mV}$; therefore, the VOC could be designed with a smaller range and thus the bitdepth could be reduced as well, while maintaining the same performance.

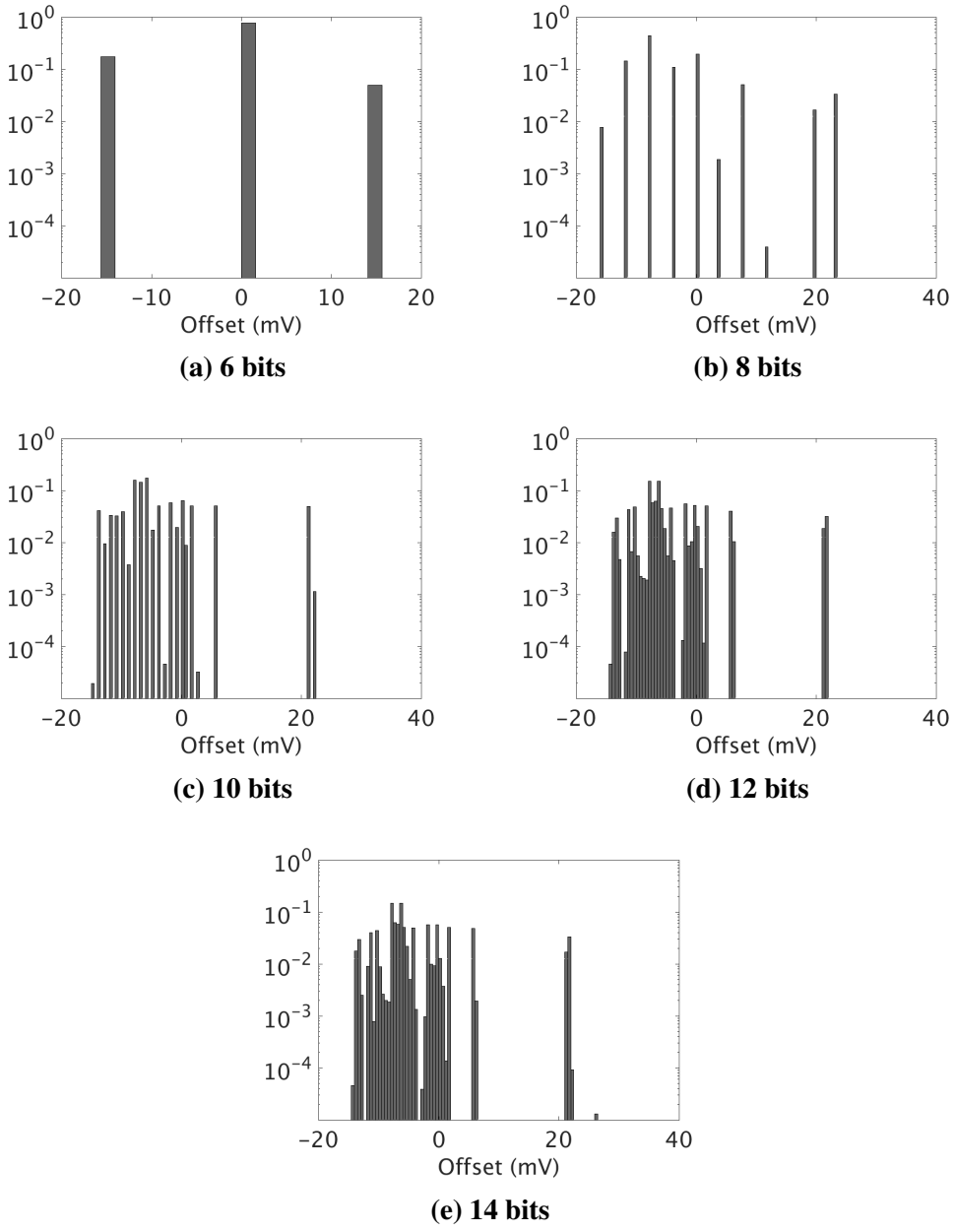
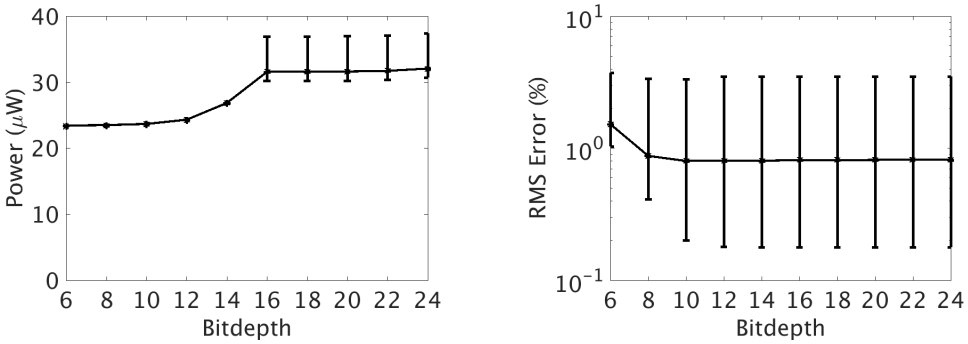


Fig. 10 VOC offset voltages for various resolutions

4.4.2 ADC Resolution

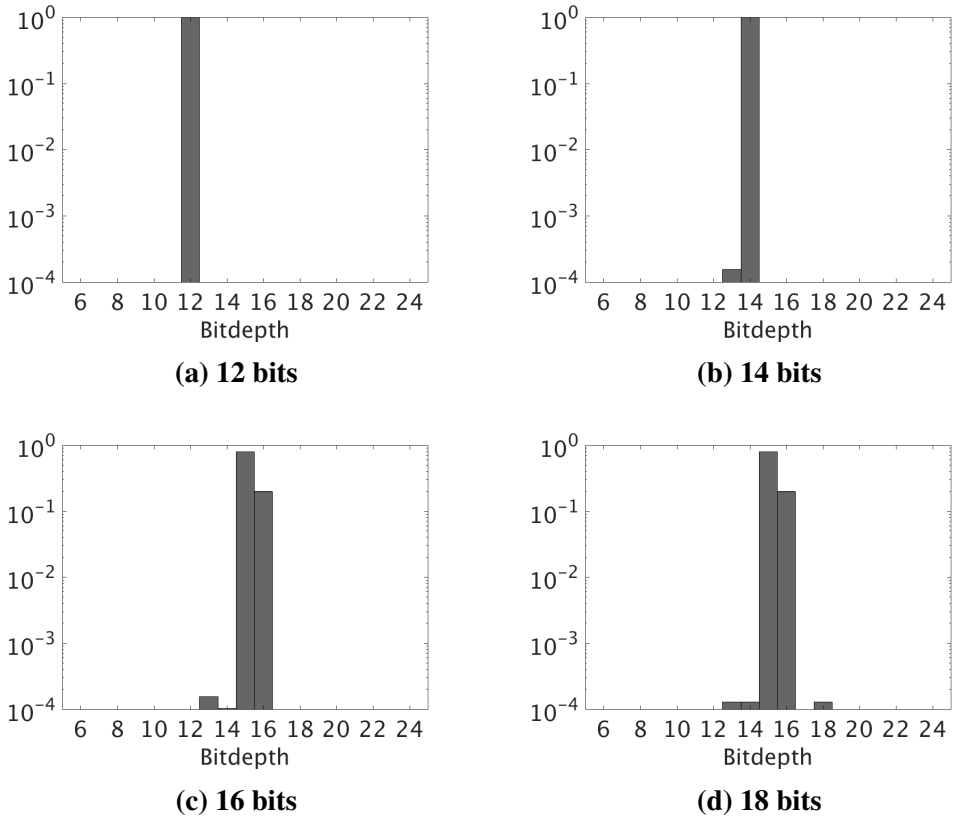
The ADC maximum bitdepth is varied from 6 to 24 bits. Figure 11 shows the impact of the ADC bitdepth. In Fig. 11a, it is notable that after 16 bits the power no longer increases as a function of 2^N; this is because for most of the signals, maintaining the 1-µV resolution, up to 17 bits would be required, as discussed in Section 2.3.3.

Figure 12 also shows this effect, increasing from 12 to 18 bits; the majority of the bitdepths settle on 14 to 16 bits. This effect is coupled to the LNA gain since it is used to determine the bitdepth required; as shown in Fig. 13, most of the time, the LNA is set between 20–50 dB.



(a) Power **(b) RMS Error**

Fig. 11 Performance impacts of ADC resolution



(a) 12 bits **(b) 14 bits**

(c) 16 bits **(d) 18 bits**

Fig. 12 ADC bitdepths selected

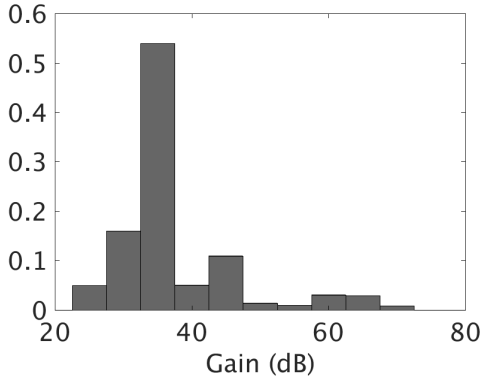


Fig. 13 LNA gain settings

Table 4 summarizes the impact and identifies the expected bitdepth range required to meet a 6σ performance objective. In this case, the range would be 13 to 17 bits. This would indicate that adding additional bits to the ADC would not gain the

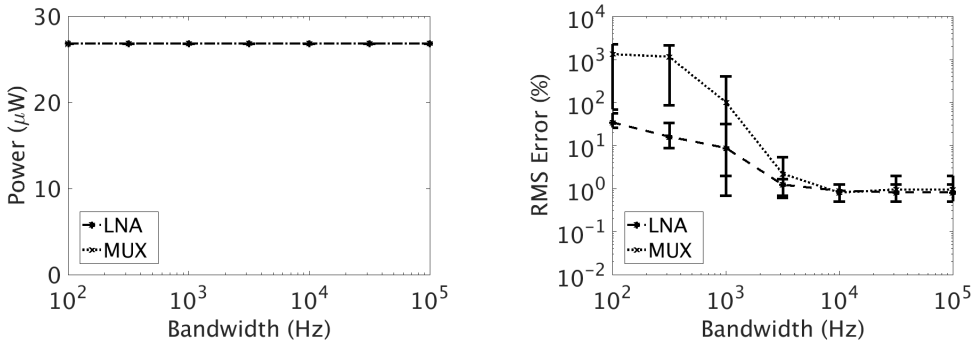
system much, although it would increase the complexity of the ADC substantially.

Table 4 ADC bitdepth summary

Max Bitdepth	Power (µW)	RMS Error (%)	Selected Bitdepth (bits)		6σ Range (bits)
			Mean	STDEV	
6	23.43	1.56	6.00	0.00	$6-6$
8	23.49	0.88	8.00	0.00	$8-8$
10	23.67	0.80	10.00	0.00	$10-10$
12	24.31	0.81	12.00	0.00	$12-12$
14	26.84	0.81	14.00	0.01	$13-15$
16	31.56	1.25	15.25	0.44	$13-17$
18	31.58	0.82	15.25	0.44	$13-17$
20	31.67	0.82	15.26	0.44	$13-17$
22	31.71	0.82	15.26	0.44	$13-17$
24	32.06	0.82	15.26	0.45	$13-17$

4.4.3 Bandwidth

The bandwidth of the AFE components will be very important to guarantee the full signal can be measured; therefore, each component will need at least 100 Hz of bandwidth. Only 2 of the AFE components model their bandwidth, the LNA and MUX. These bandwidths were simulated from 100 Hz to 100 kHz. Figure 14 shows the bandwidth impact for the LNA and MUX for a 4 channel system. As one would expect, there is almost no impact on power. For both the LNA and VOC, the bandwidths less than 10 kHz appear to have a large impact on the error. For the VOC, this is amplified because the channels are time multiplexed together, effectively modulating those to a higher frequency. Therefore, this component would need to be designed to have significant headroom to prevent this from becoming an issue.

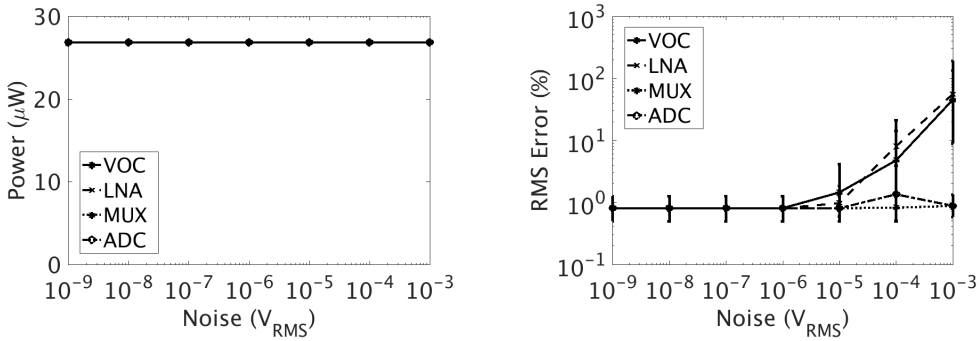


(a) Power **(b) RMS Error**

Fig. 14 Performance impacts of LNA and MUX bandwidth

4.4.4 Noise

Another major contributor to the system performance is the noise the system adds to the signals. This has been modeled in each of the 4 AFE components as flicker and white noise. The results have been plotted in Fig. 15, which shows the impact on the LNA, VOC, MUX, and ADC. The 2 components that are interacting with the unamplified signal have the greatest impact on the signal fidelity. Since the system is targeting a 1-μV resolution, the LNA and VOC components need to have input/output noise that is less than that, as evidenced by Fig. 15b, where the signal reconstruction error increases drastically above 1 μV. Unlike the LNA and VOC, the MUX and ADC noise is less of an issue since the signal has already been amplified only at the extreme end of the simulations; at 1 mV RMS, the noise does appear to impact the performance, but it is still less than 1%.

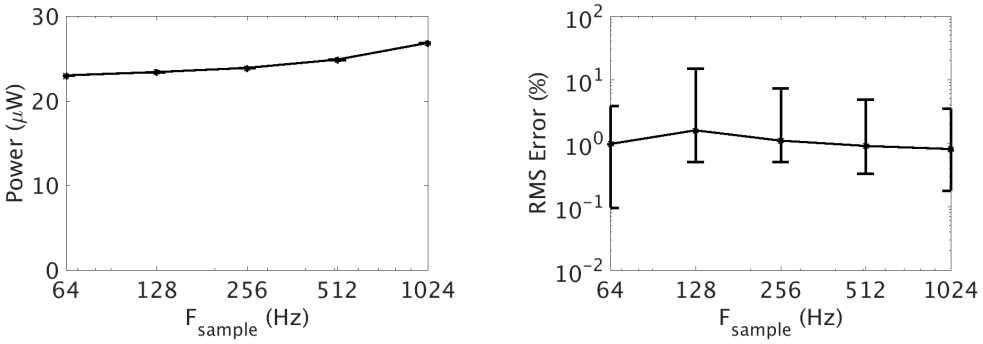


(a) Power **(b) RMS Error**

Fig. 15 Performance impacts of VOC, LNA, MUX, and ADC noise

4.4.5 Sampling Frequency

The final parameter in the system is the sampling frequency. For these simulations, the lower bound was set at 64 Hz, which matches the adjustment frequency, and the upper bound is 1024 Hz. Figure 16 shows the system performance across these sampling frequencies. As one would expect, the power increases with the sampling frequency, but there is not much of an impact on the signal fidelity above 256 Hz. So therefore, the sampling frequency will likely just depend on the application and available power and not on a specific error target.



(a) Power **(b) RMS Error**

Fig. 16 Performance impacts of sampling frequency

5. Conclusions

In this work, a new architecture to perform EEG recording has been presented. While this work focused on the EEG applications, this architecture can be used for other sensing applications where self-powered sensors would be desirable, such as for Internet of Things systems. The presented architecture is capable of low-power operation while maintaining a similar signal fidelity, within 1%, as regular full-power system, while consuming less than 1% the power of the baseline system.

This architecture accomplishes this by using an adaptive feedback to control the gain and offset of the AFE, which ensures the amplifiers are not saturated and clipping the signal. Without this adaptive feedback, extremely low-voltage operation would not be possible due to the amplifiers.

Additionally, this work presented an evaluation of the major parameters of each component in the system. This shows that the bandwidth and noise of the AFE

will need to be designed carefully to ensure proper operation, while the adjustment frequency, sampling frequency, and ADC bitdepth, as long as they were sufficiently high to meet the requirements of the application, do not have a large impact on the performance of the system for the algorithms and application presented in this work.

This architecture will enable real-world EEG recording, which will help enable neuroscientists to study brain activity outside of the laboratory setting.

6. References

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List of Symbols, Abbreviations, and Acronyms

ADA	adaptive data acquisition
ADC	analog-to-digital converter
AFE	analog frontend
DAC	digital-to-analog converter
DC	direct current
DSP	digital signal processor
ECoG	electrocorticography
EEG	electroencephalogram
LNA	low-noise amplifier
MUX	multiplexer
RF	radio frequency
RMS	root mean square
SubVt	subthreshold
TEG	thermoelectric generator
VGA	variable gain amplifier
VOC	voltage offset controller

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